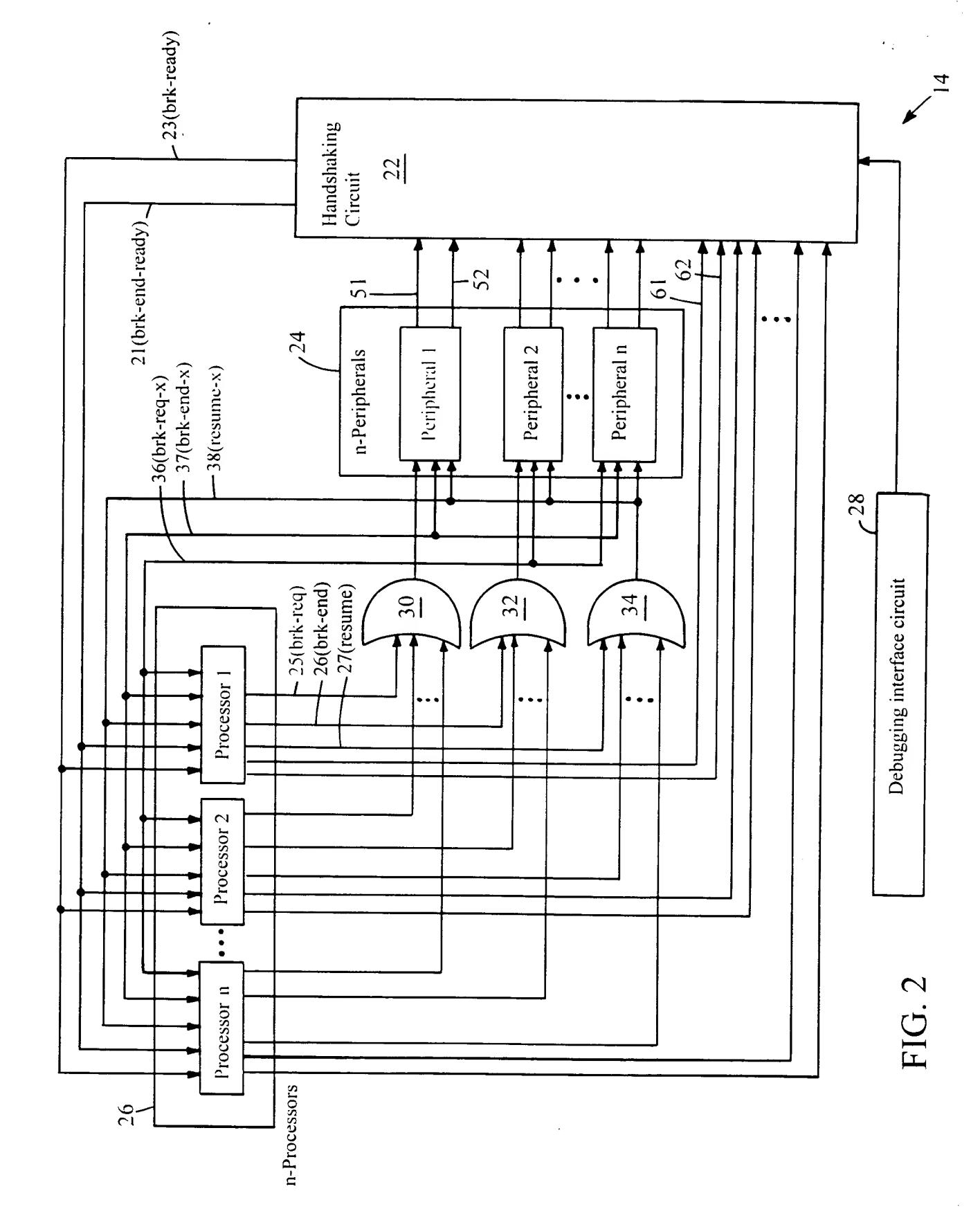


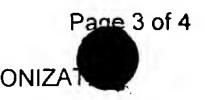
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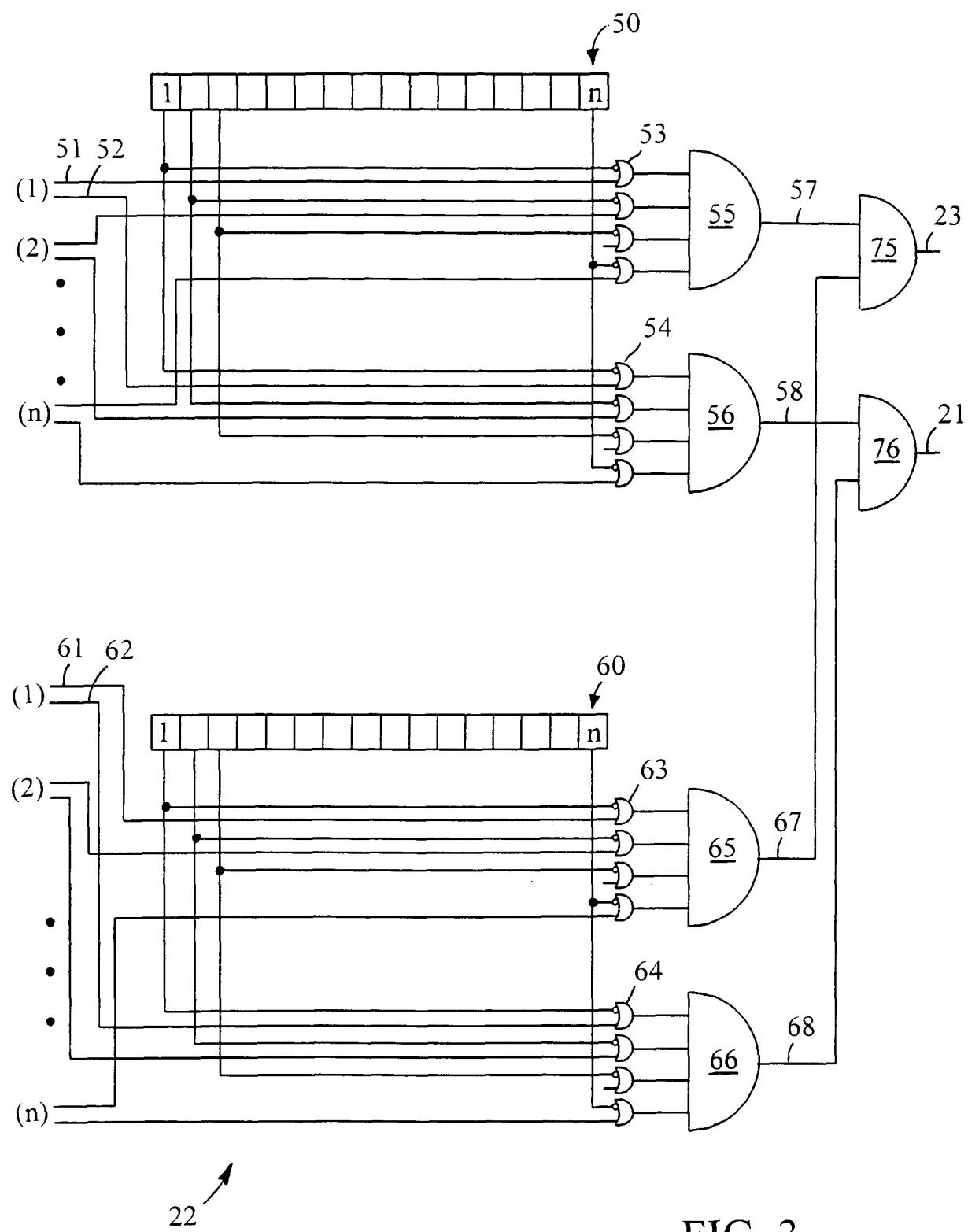


FIG. 3

SY ON-CHIP BREAKPOINT SYNCHRONIZATI

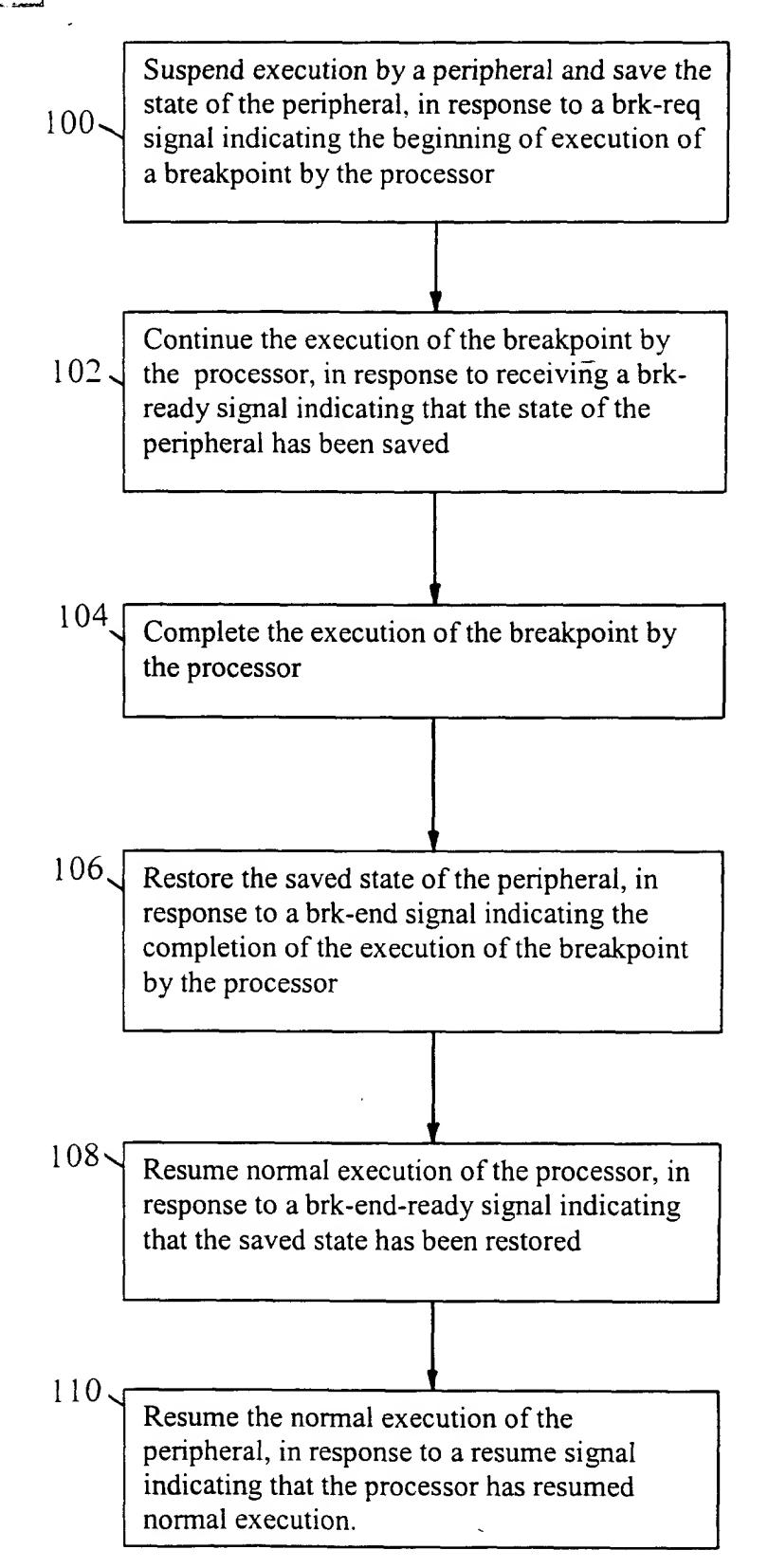


FIG. 4